

FIG. 1  
PRIOR ART

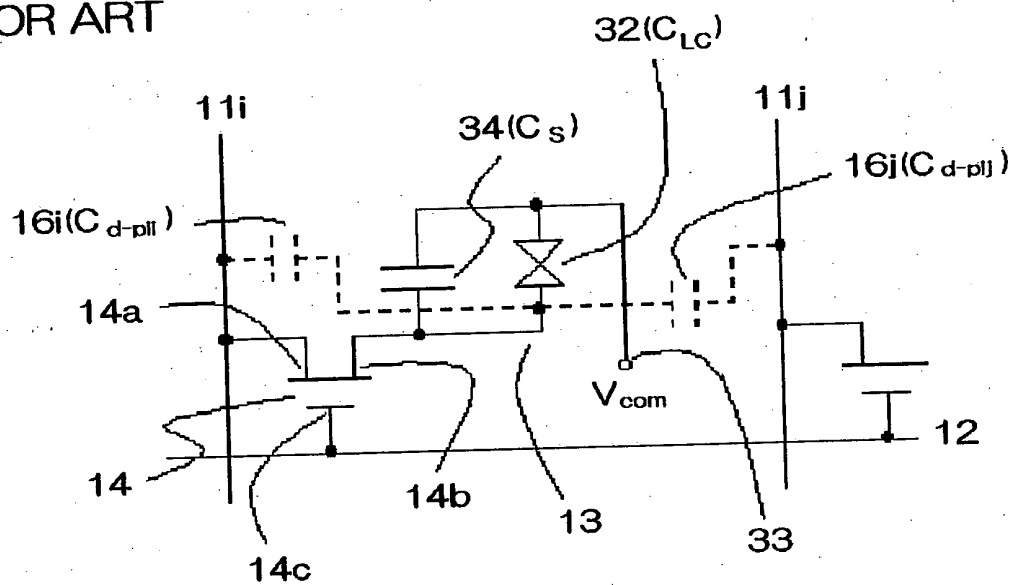


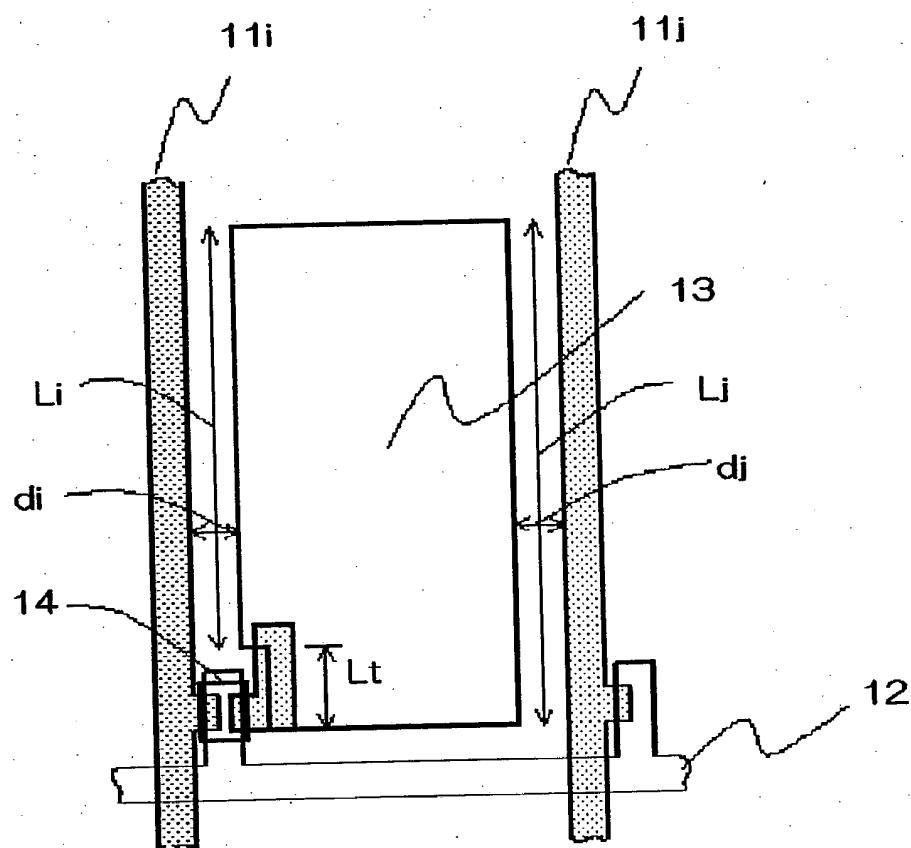
FIG. 2  
PRIOR ART

FIG. 3A  
PRIOR ART

	11i	11j	11k	11l
12i	+	+	+	+
12j	-	-	-	-
12k	+	+	+	+
12l	-	-	-	-

Nth PERIOD

FIG. 3B  
PRIOR ART

	11i	11j	11k	11l
12i	-	-	-	-
12j	+	+	+	+
12k	-	-	-	-
12l	+	+	+	+

(N+1)th PERIOD

68260 3024060

FIG. 4A  
PRIOR ART

	11i	11j	11k	11l
12i	+	-	+	-
12j	+	-	+	-
12k	+	-	+	-
12l	+	-	+	-

Nth PERIOD

FIG. 4B  
PRIOR ART

	11i	11j	11k	11l
12i	-	+	-	+
12j	-	+	-	+
12k	-	+	-	+
12l	-	+	-	+

(N+1)th PERIOD

13

FIG. 5A  
PRIOR ART

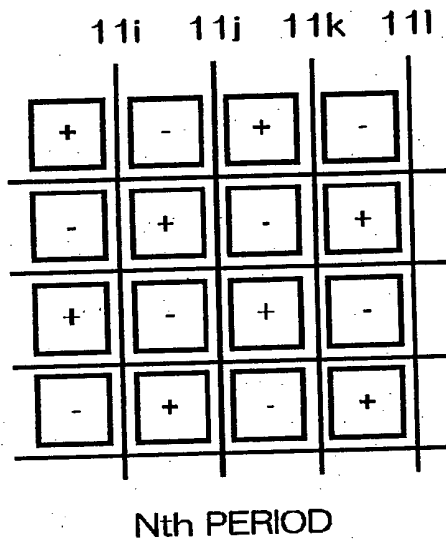


FIG. 5B  
PRIOR ART

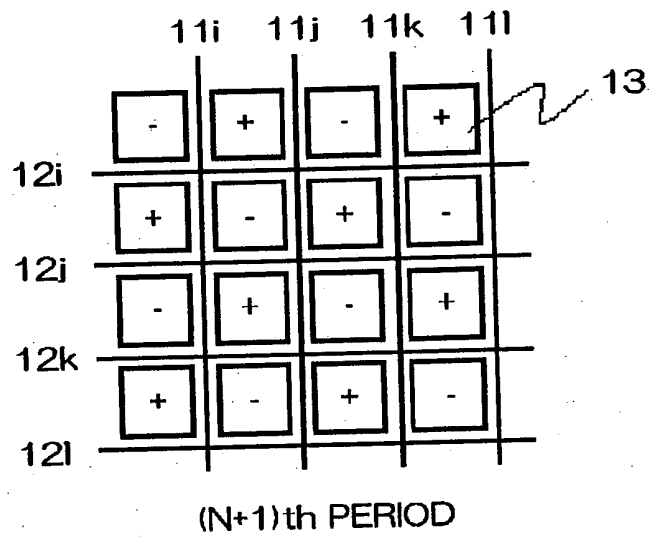
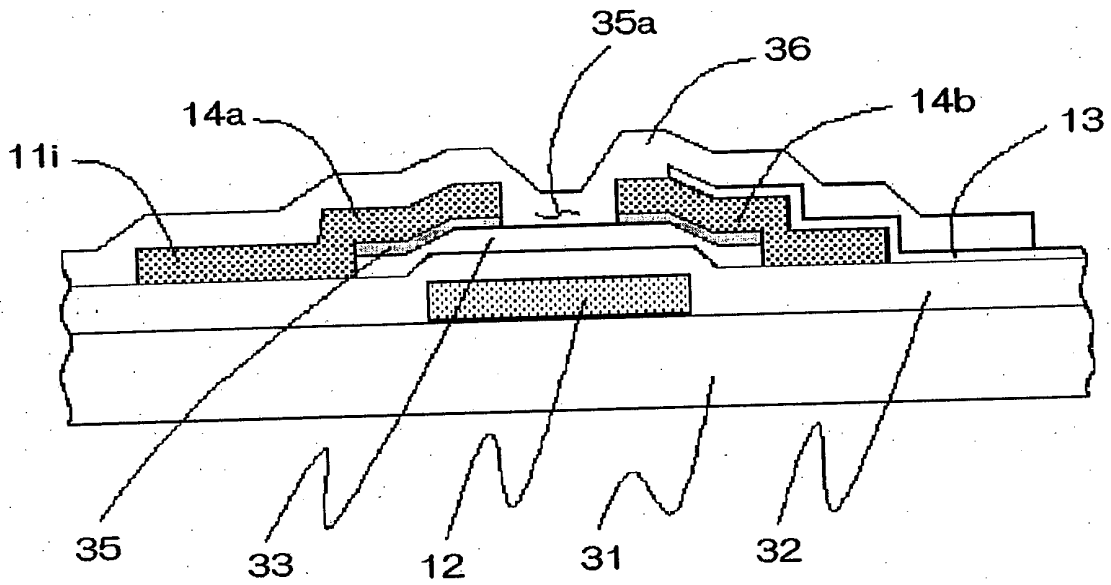


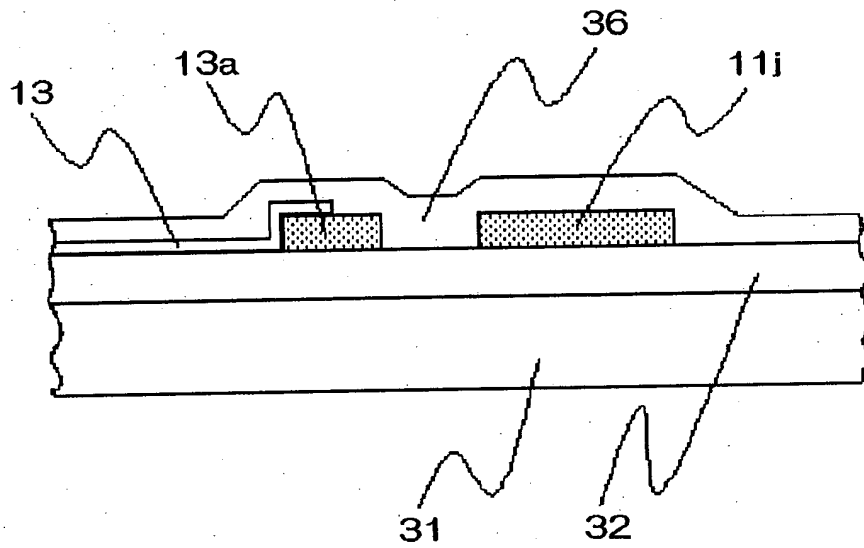


FIG. 7



60260-5040160

FIG. 8



652260" 50440460



FIG. 9

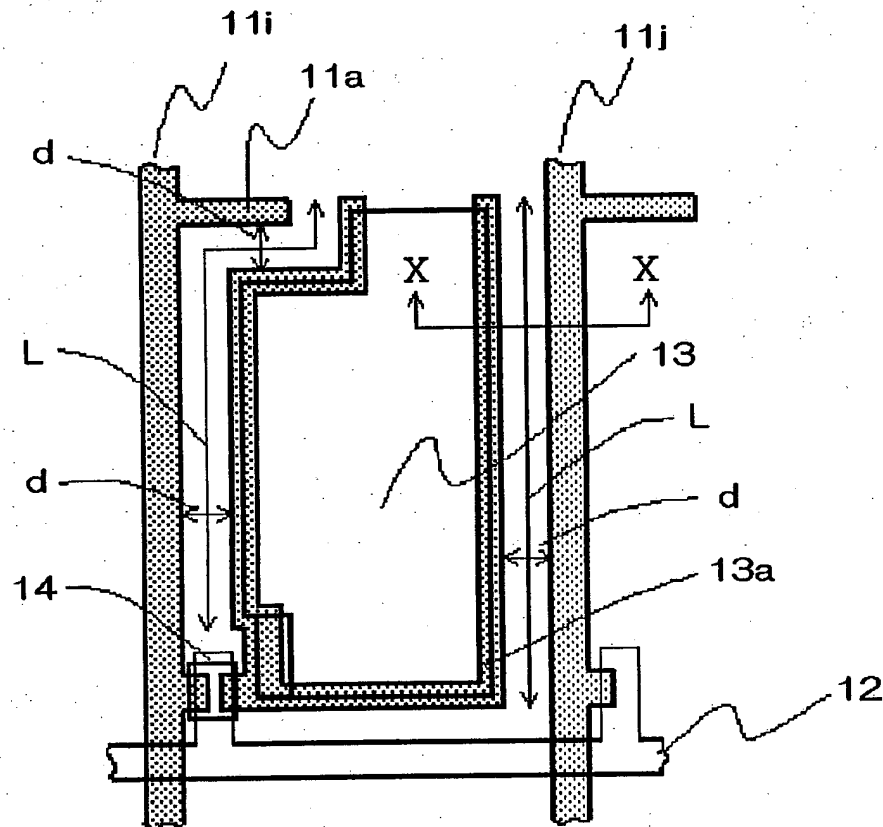


FIG. 10

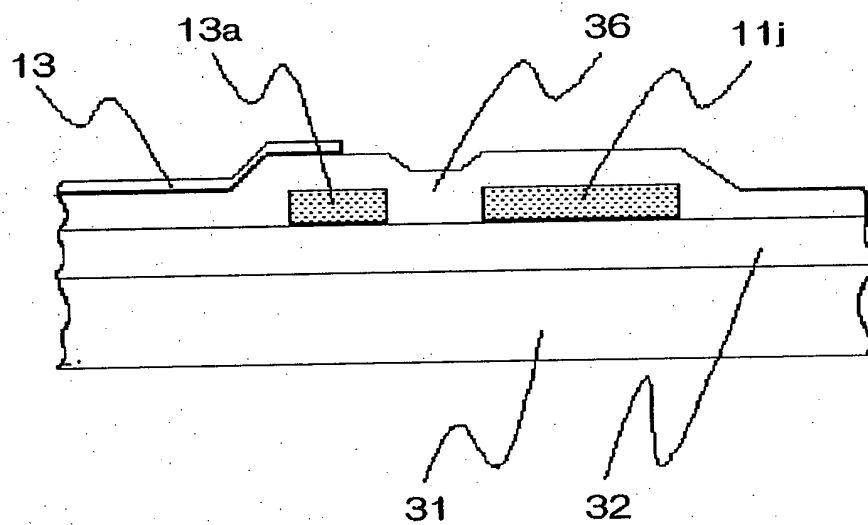


FIG. 11

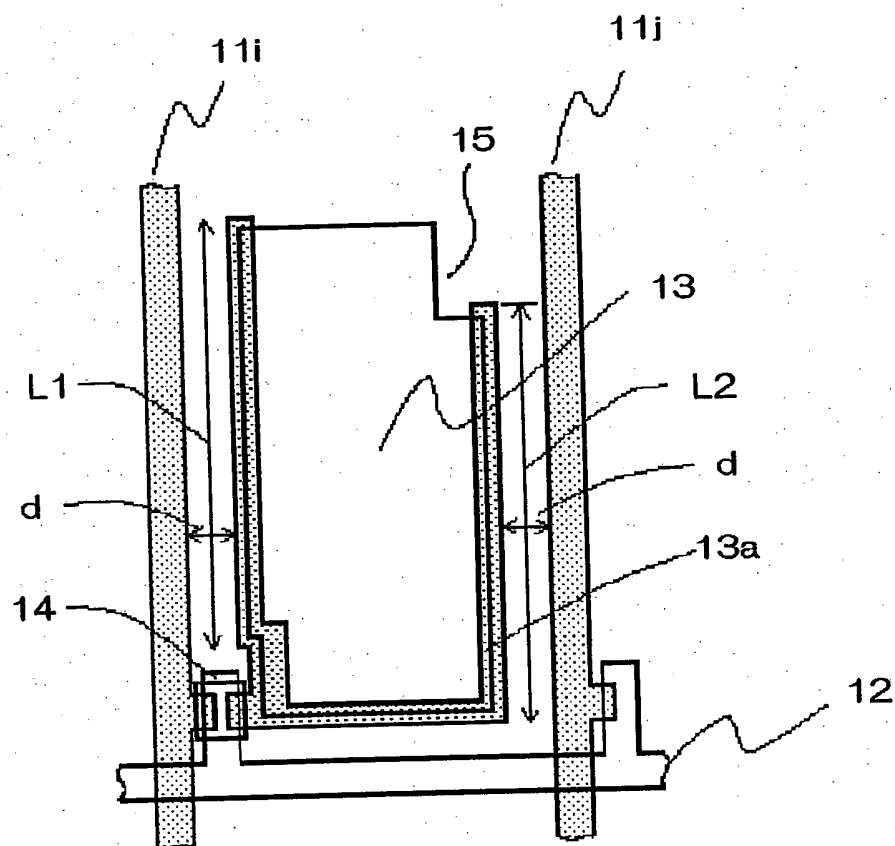


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 10 with a top layer 11. A central region 12 contains a series of nested rectangular structures 13. The top layer 11 has openings 11i and 11j. A layer 14 is at the bottom. Dimensions d and L are indicated for various layers and structures.

FIG. 13

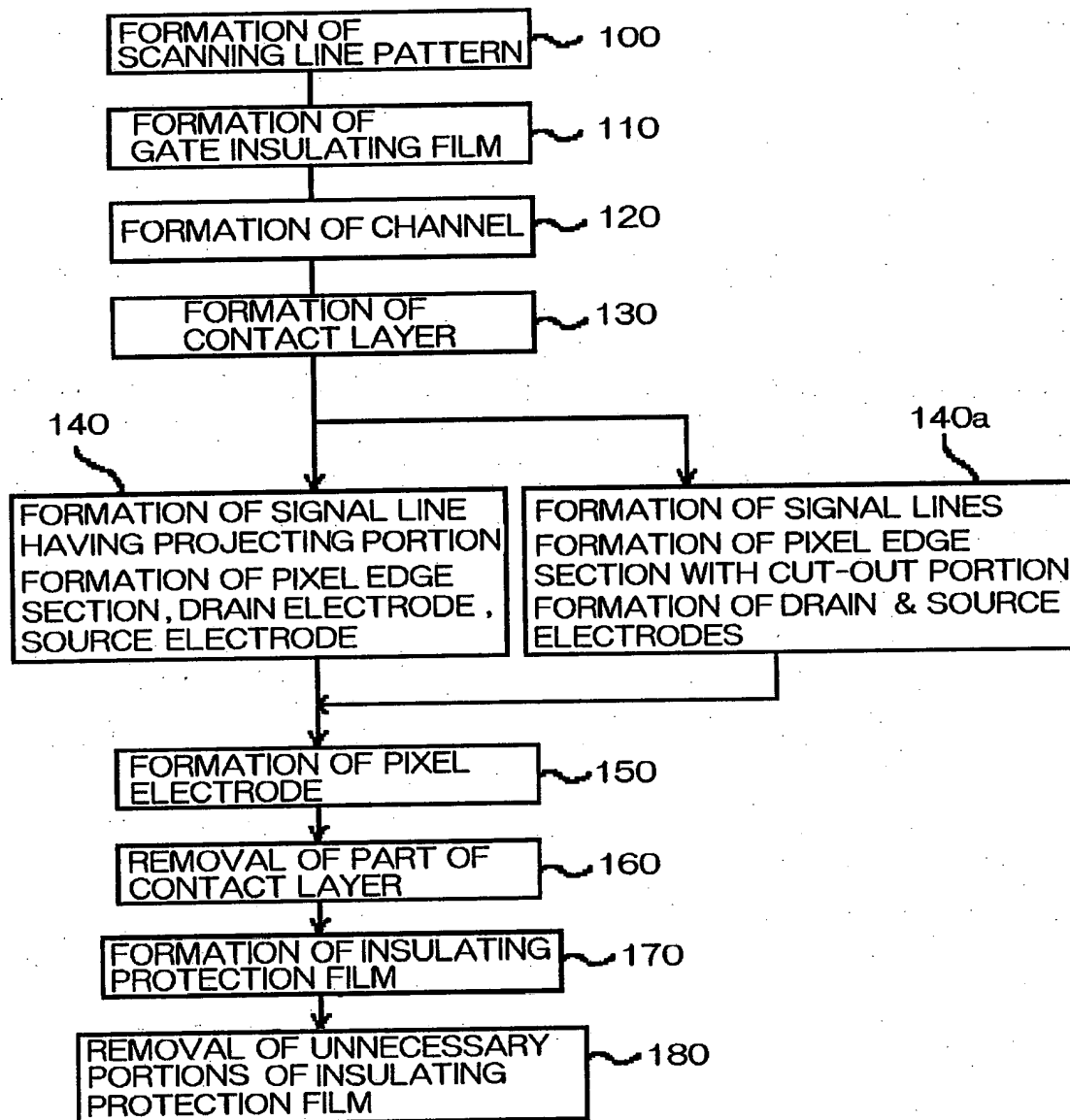


FIG. 14

